FIG 1

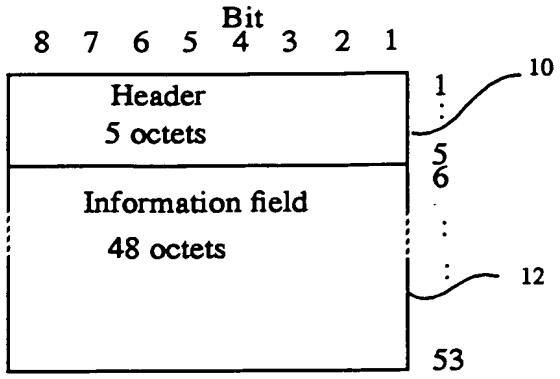


FIG 2

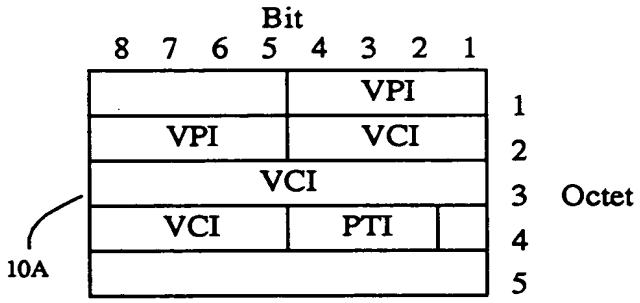


FIG 3

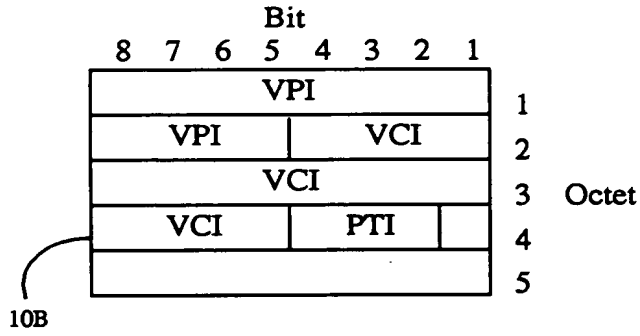


FIG 4

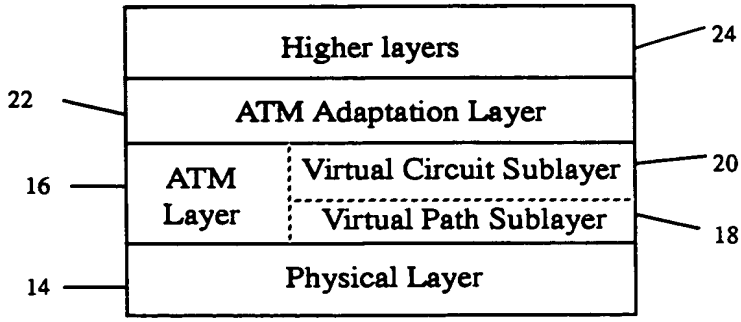


FIG5

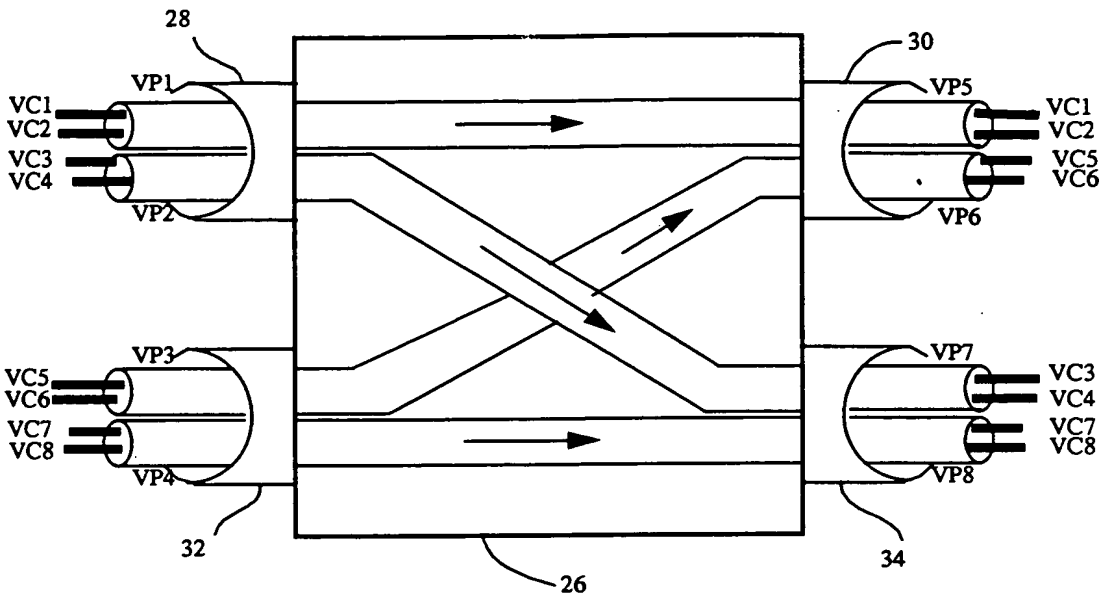

28
30
VP1
VP5
VC1
VC2
VC3
VC4
VP2
VC1
VC2
VC5
VC6
VP6
VP3
VP7
VC5
VC6
VC3
VC4
VC7
VC8
VP4
VC7
VC8
VP8
32
34
26

FIG 6

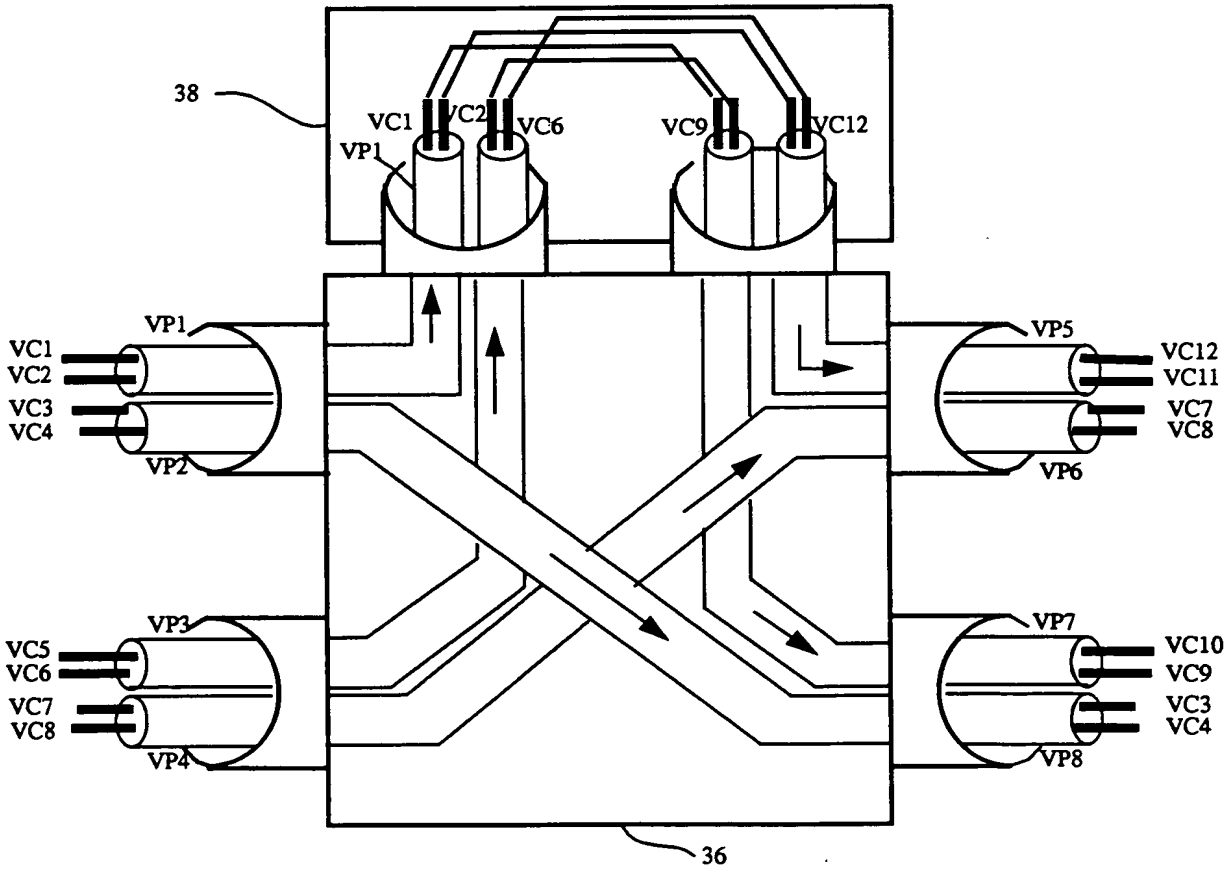

38
VC1
VC2
VC6
VC9
VC12
VP1
VP1
VP5
VC1
VC2
VC12
VC11
VC3
VC4
VC7
VC8
VP2
VP6
VP3
VP7
VC5
VC6
VC10
VC9
VC7
VC8
VC3
VC4
VP4
VP8
36

FIG 7

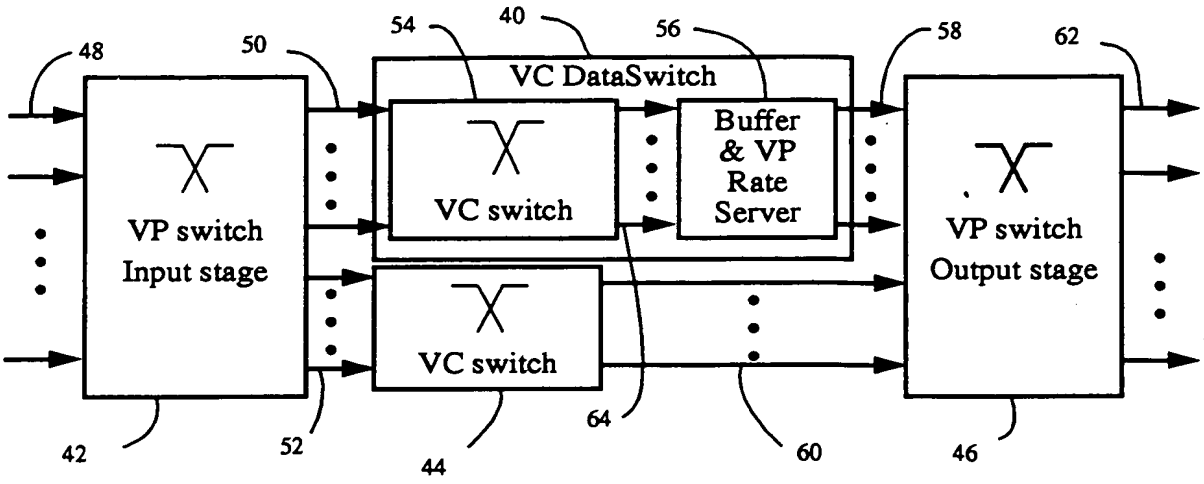

48
50
54
40
56
58
62
VC DataSwitch
VP switch
Input stage
VC switch
Buffer
& VP
Rate
Server
VP switch
Output stage
VC switch
42
52
44
64
60
46

FIG 8

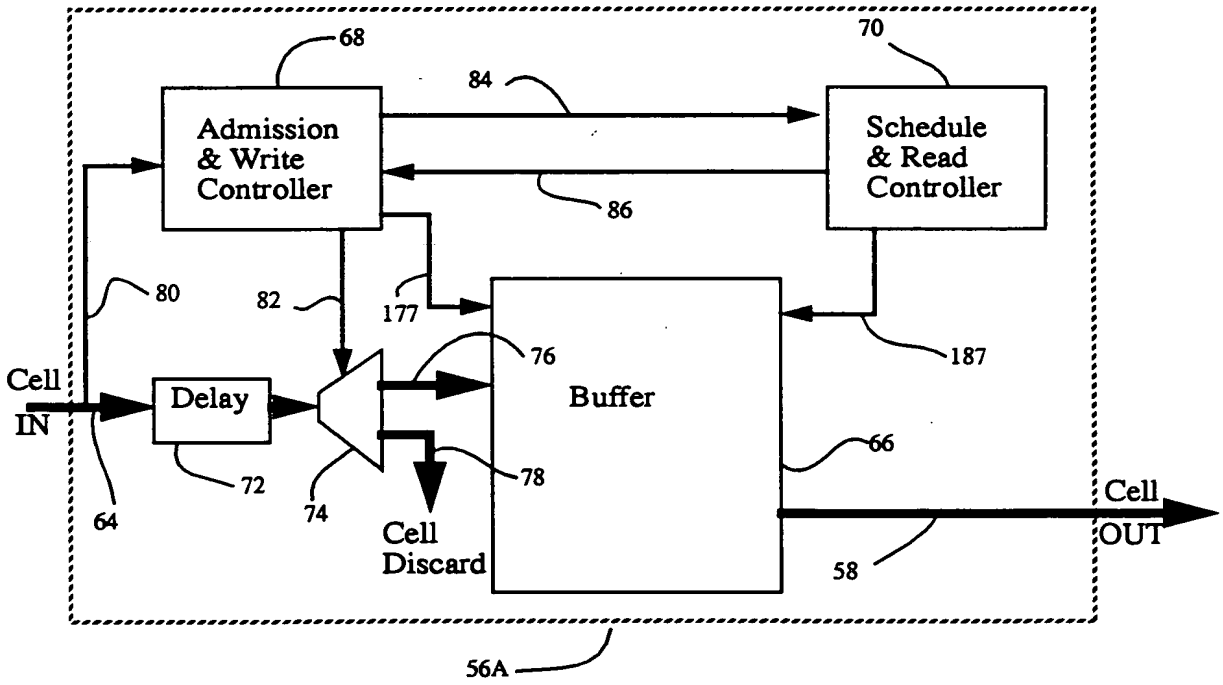

68
70
84
Admission
& Write
Controller
Schedule
& Read
Controller
86
80
82
177
187
76
Cell
IN
Delay
Buffer
66
72
74
78
64
Cell
Discard
Cell
OUT
58
56A

FIG 9

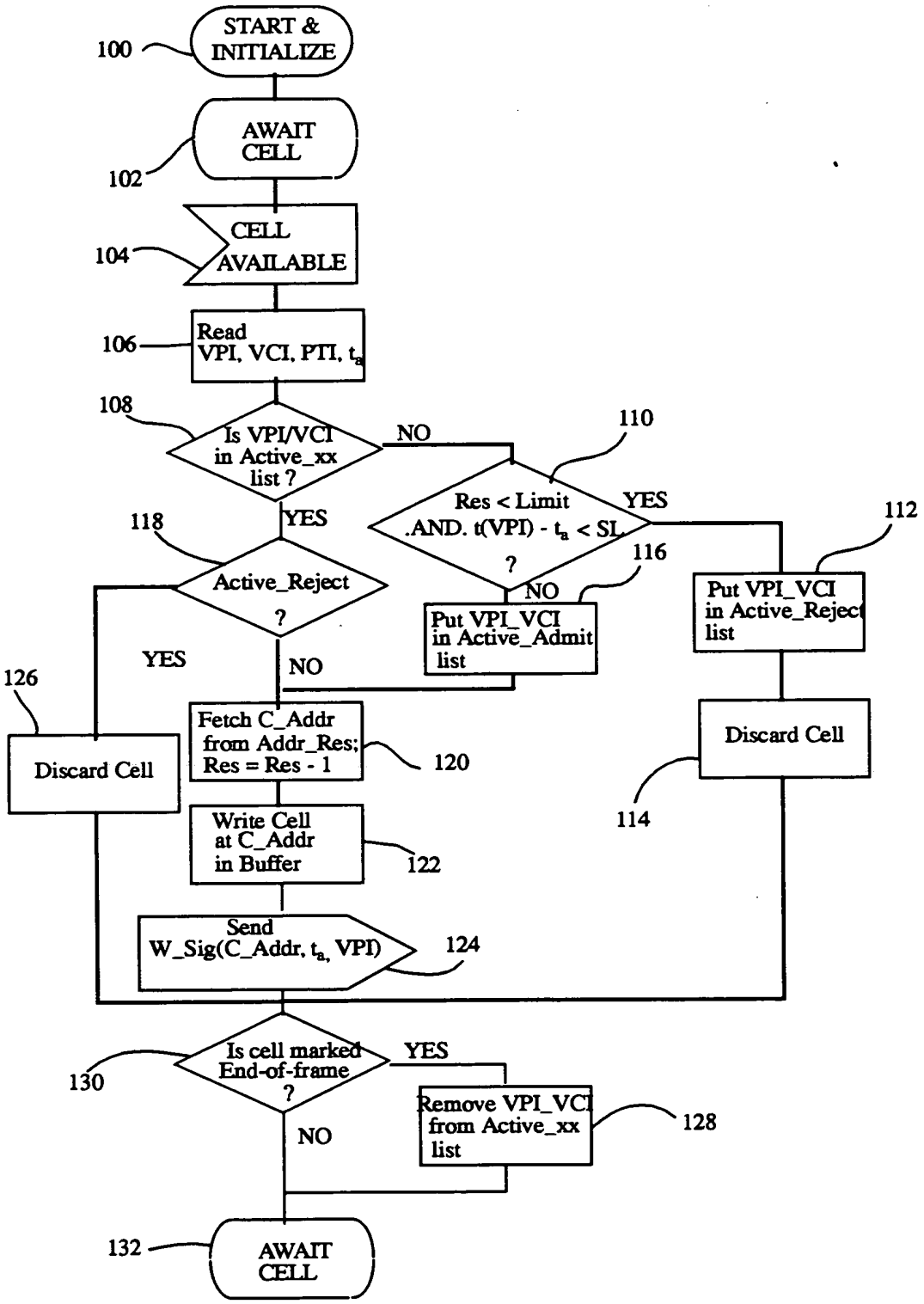

START & INITIALIZE
100
AWAIT CELL
102
CELL AVAILABLE
104
Read VPI, VCI, PTI, t_a
106
Is VPI/VCI in Active_xx list ?
108
NO
YES
Res < Limit .AND. t(VPI) - t_a < SL ?
110
YES
NO
Active_Reject ?
118
YES
NO
Put VPI_VCI in Active_Admit list
116
Put VPI_VCI in Active_Reject list
112
Discard Cell
126
Fetch C_Addr from Addr_Res; Res = Res - 1
120
Discard Cell
114
Write Cell at C_Addr in Buffer
122
Send W_Sig(C_Addr, t_a, VPI)
124
Is cell marked End-of-frame ?
130
YES
NO
Remove VPI_VCI from Active_xx list
128
AWAIT CELL
132

FIG 10

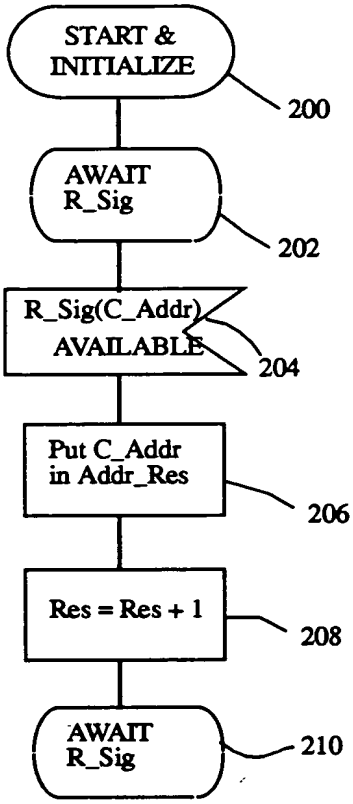


FIG 10A

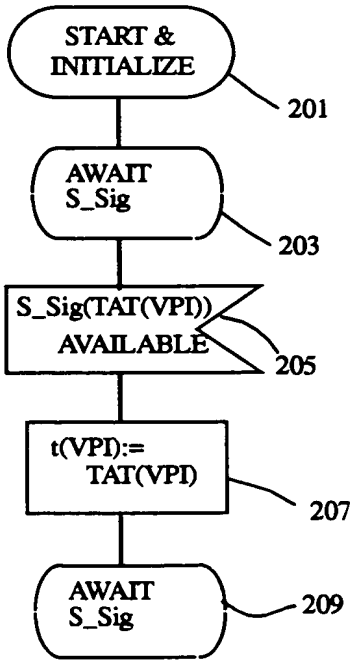


FIG 11

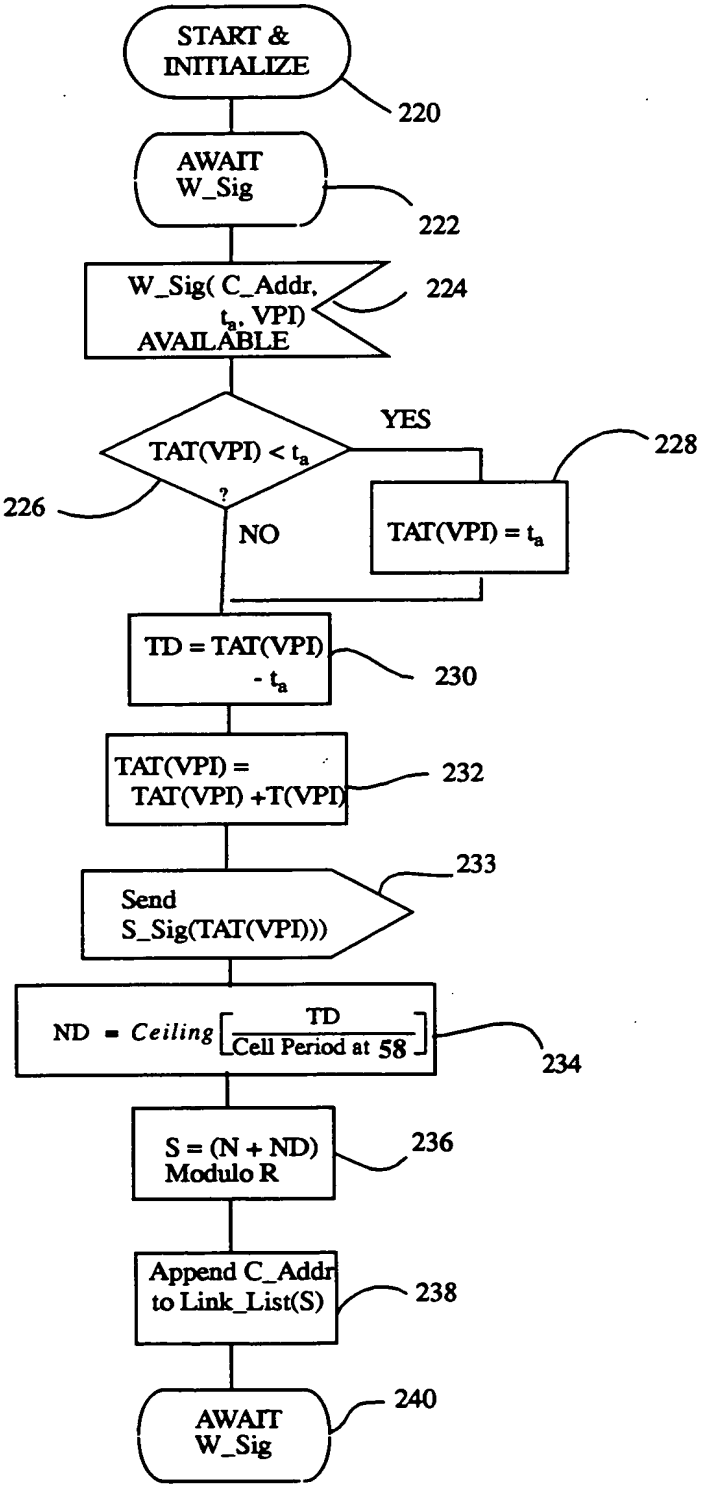
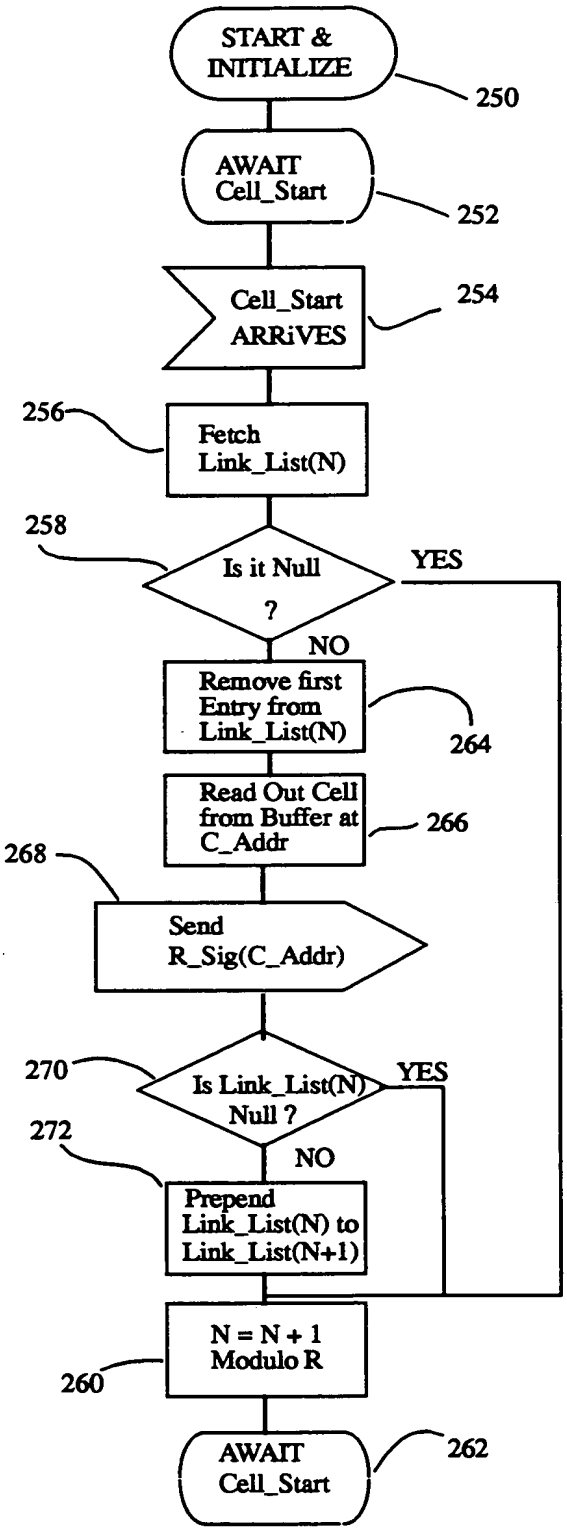

START & INITIALIZE
220
AWAIT W_Sig
222
W_Sig(C_Addr, t_a, VPI) AVAILABLE
224
TAT(VPI) < t_a ?
YES
NO
226
228
TAT(VPI) = t_a
TD = TAT(VPI) - t_a
230
TAT(VPI) = TAT(VPI) +T(VPI)
232
Send S_Sig(TAT(VPI))
233
ND = Ceiling [TD / Cell Period at 58]
234
S = (N + ND) Modulo R
236
Append C_Addr to Link_List(S)
238
AWAIT W_Sig
240

FIG 12


START & INITIALIZE
250
AWAIT Cell_Start
252
Cell_Start ARRiVES
254
256
Fetch Link_List(N)
258
Is it Null ?
YES
NO
Remove first Entry from Link_List(N)
264
Read Out Cell from Buffer at C_Addr
266
268
Send R_Sig(C_Addr)
270
Is Link_List(N) Null ?
YES
272
NO
Prepend Link_List(N) to Link_List(N+1)
N = N + 1 Modulo R
260
AWAIT Cell_Start
262